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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,541	09/19/2003	Jean-Marc Bachot	TI-27700A	4292

23494 7590 07/29/2004

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
ELMORE, STEPHEN C	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,541	BACHOT ET AL.	
	Examiner	Art Unit	
	Stephen Elmore	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-26* is/are allowed.

6)☒ Claim(s) *28-37,39,40,43 and 50-61* is/are rejected.

7)☒ Claim(s) *27, 38, 41, 42, and 44-49* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/410,772.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/19/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 were canceled and claims 19-61 were added by the preliminary amendment.

2. Claims 19-61 are presented for examination.

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Information Disclosure Statement

4. The information disclosure statement filed September 19, 2003 contains non-patent publications identified "CA-CY" which were not provided with the instant patent application, and whose identification is incomplete in that these items represent copending patent applications which have not been fully identified by their patent office Serial Numbers, therefore, without the serial numbers they could not be located or considered. These references have been "lined-through" to show their status.

Claim Objections

5. Claims 27 and 61 are objected to because of the following informalities:

a. claims 27 and 61, the term "address" is expressed in non-idiomatic English.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 31, 39, 40 and 43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. The claims are indefinite because as to the following language:

a. claim 31, "said circuitry";

b. claim 39, "the hold time" and "the address bus";

c. claim 40, "the hold time," "the address bus" and "the bus";

d. claim 43, "the system clock";

these claims recite the indicated limitations mentioned above, however, there is insufficient antecedent basis for these limitations in the respective claim.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claim 28 is rejected under the judicially created doctrine of obvious-type double patenting as being unpatentable over claim 27 of US Patent No. 6,629,223. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Claim 27 of US Patent No. 6,629,223 contains every element of claim 28 of the instant application and as such **anticipates** claim 28 of the instant application.

"A latter patent claim is not patentably distinct from an earlier patent claim if the latter claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obvious-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obvious-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Furthermore,

Claim 27 of US Patent 6,629,223 is reproduced:

27. An electronic system, comprising:

at least one input/output device; and

an integrated circuit, coupled to the at least one input/output device, and comprising:

functional circuitry for executing logical operations upon digital data signals in a synchronous fashion [according to an internal clock signal];

[power distribution circuitry, coupled to a battery, for distributing power to the functional circuitry;] and circuitry coupled to a memory core in said integrated circuit for accessing said memory core more than once in a single clock cycle wherein self-timing logic provides signals that facilitate said accessing.

and,

Claim 28 from the instant application is reproduced:

28. An electronic system, comprising:

at least one input/output device; and

an integrated circuit, coupled to the at least one input/output device, and comprising:

functional circuitry for executing logical operations upon digital data signals in a synchronous fashion; and

[access] circuitry coupled to a memory core in said integrated circuit for accessing said memory core more than once in a single clock cycle wherein self-timing logic provides signals that facilitate said accessing.

Where, in the above claim comparisons, any differences between the two claims are shown in [brackets] and note that there are only two kinds of differences.

First, prior claim 27 contains every element of claim 28 of the instant application except for the presence of "[access] circuitry" in claim 28, however, this difference is not patentably distinct because the corresponding "circuitry" element in claim 27 is inherently "access circuitry" and therefore equivalent, because this circuitry accesses the memory core as claimed, therefore, although not identical in language these two limitations are equivalent, not patentably distinct.

Second, prior claim 27 contains the features an "internal clock signal" and "power distribution circuitry" with attendant functionality which makes claim 27 a "species" of the "genus" claim 28, because it is more specific and because claim 28 being broader is a "genus" in relation to claim 27 and does not contain these features, therefore, patent application claim 28 is a genus which is **anticipated** by patent claim 27 species.

Humans are a species of the animal genus. Our case law firmly establishes that a later genus claim limitation is anticipated by, and therefore not patentably distinct from, an earlier species claim. *In re Berg*, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 1053, 29 USPQ2d 2010, 2016(Fed. Cir. 1993); *In re Gosteli*, 872 F.2d 1008, 1010, 10 USPQ2d 1614, 1616(Fed. Cir. 1989); *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 782, 227 USPQ 773, 779 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d at 944, 214 USPQ at 767 (C.C.P.A. 1982)." ELI LILLY AND COMPANY v BARB LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 28 and 30-37, 50 and 51-61 are rejected under 35 U.S.C. 102(b) as being anticipated by Garde et al., US Patent 5, 685,005 and Garde, US Patent 5,396,608, which is incorporated by reference in USP 5,685,005 at col. 4, line 59, therefore, this is a two reference 102(b) rejection due to the incorporation by reference, i.e., the two references are taken together for all their teachings.

Garde ('005) and Garde ('608) teaches the claimed electronic system (claim 28), memory module (claim 37), and processing apparatus (claim 52), comprising:

where the following limitations are taught by citations from the first reference, Garde ('005), unless otherwise noted,

Claim 28,

a. at least one input/output device (14); and an integrated circuit (10), coupled to the at least one input/output device, and comprising: functional circuitry for executing logical operations upon digital data signals in a synchronous fashion; and access circuitry coupled to a memory core in said integrated circuit for accessing said memory core more than once in a single clock cycle wherein self-timing logic provides signals that facilitate said accessing, is taught as the digital signal processor 10, see Fig. 1, and see col. 5, line 66 - col. 6, line 21, and note the two separate and independent accesses to memory bank 28 during a single clock cycle, taught at col. 6, lines 15-17, where the claimed "self-timing logic" feature is taught to the extent it is claimed by the clock cycle being divided into two phases which facilitate accessing of the memory core, and which is "self-timing" to the extent that the two clock phases are used solely for accessing the DSP's own memory banks, that is, for itself thereby meeting the limitation as far as it is actually claimed;

b. claim 30, wherein said memory core is part of a dual-access RAM -- see col. 4, line 41, each bank is dual ported;

c. claim 31, wherein said memory core and said circuitry combine to form a multiple access memory core -- because memory banks (cores) 28 and 30 can be accessed multiple times;

d. claim 32, wherein said access circuitry is embodied in an electronic device coupling a memory interface unit to said memory core -- because the buses inherently interface with the memory bank cores;

e. claim 33, wherein said electronic system is a digital signal processor -- DSP 10;

f. claim 34, wherein said memory core is part of a core of a processor -- memory cores 28 and 30 are a part of DSP 10 which is also a core;

and as to,

g. claim 35, wherein addresses accessed in said memory core are adjacent addresses;

and

h. claim 36, wherein address accessed in said memory core are non-adjacent addresses, both of these limitations are met by the references taken together, see Garde ('608), Figs. 4A and 4B, showing addresses of stored data which are both adjacent and non-adjacent (discontiguous) and, only accessible by alternate addressing, and see col. 4, line 48 - col. 5, line 40;

Claim 37,

i. a memory interface unit; a memory core; and circuitry for coupling said memory interface unit to said memory core and enabling access to said memory core at least two times in a single clock cycle, is taught as the multiplexers 86 and 88, see Fig. 1, and see col. 3, line 8 - col. 4, line 65, and note the two separate and independent accesses to memory bank 28 during a single clock cycle, taught at col. 6, lines 15-17;

and as to,

j. claim 50, wherein addresses accessed in said memory core are adjacent addresses;

and

k. claim 51, wherein address accessed in said memory core are non-adjacent addresses, both of these limitations are met by the references taken together, see Garde ('608), Figs. 4A and 4B, showing addresses of stored data which are both adjacent and non-adjacent (discontiguous) and, only accessible by alternate addressing, and see col. 4, line 48 - col. 5, line 40;

Claim 52,

l. a processing engine (12), and a processor backplane coupled to said processing engine (busses and interfacing logic), said processor backplane comprising a memory module, said memory module (16), comprising: a memory interface unit (multiplexers 86 and 88); a memory core (28 and 30); and circuitry for coupling said memory interface unit to said memory core and enabling access to said memory core at least two times in a single clock cycle, is taught as the two separate and independent accesses to memory bank 28 during a single clock cycle, taught at col. 6, lines 15-17;

m. claim 53, wherein a bus couples said memory module to said processing engine -- busses 32, 34, 36;

n. claim 54, wherein said processor backplane further comprises a memory cache coupled to said processing engine -- cache 20;

o. claim 55, wherein said processor backplane further comprises at least one peripheral device coupled to said processing engine -- I/O processor 14;

p. claim 56, wherein said processor backplane further comprises an external interface coupled to said processing engine -- external port 18;

q. claim 57, a processing core coupled to a memory management unit is inherent (not shown, but necessarily present because access to memory 16 by the various processor is managed;

r. claim 58, core processor 12 is a cpu so far as it is claimed;

s. claim 59, an instruction buffer unit (82); a program flow unit (70); an address data flow unit (66 and 68); and a data computation unit (62) coupled to said instruction buffer unit, said program flow unit and said address flow unit are taught;

and as to,

t. claim 60, wherein addresses accessed in said memory core are adjacent addresses,

and

u. claim 61, wherein address accessed in said memory core are non-adjacent addresses, both of these limitations are met by the references taken together, see Garde ('608), Figs. 4A and 4B, showing addresses of stored data which are both adjacent and non-adjacent (discontiguous) and, only accessible by alternate addressing, and see col. 4, line 48 - col. 5, line 40.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Garde et al., US Patent 5, 685,005 and Garde, US Patent 5,396,608, which is incorporated by reference in USP 5,685,005 at col. 4, line 59, therefore, this is a two reference 102(b) rejection due to the

incorporation by reference, i.e., the two references taken together in view of the taking of Official Notice.

Garde et al. and Garde, taken together teaches the claimed electronic system as claimed in claim 28, however, does not teach as per claim 29 wherein said electronic system is a cellular telephone, but it is well-known in the art of the use of DSP processors to adapt or modify DSP processors to provide the general purpose processor system processing functionality required in cellular telephones because DSP processors are excellent choices for such processing requirement due to their limited instruction sets as compared to general purpose processors (i.e., the instructions are limited to the application to which they have been applied such as cellular technology), efficient use of battery life (also a consequence of the more limited instruction set which due to the smaller size of processor footprint required is more easily storable in a system ROM or FLASH and therefore draws less power, and which is therefore more desirable for portable use such as is needed in cellular technology, and such a modification of the reference is old, well-known, and would have been obvious to one of ordinary skill in the art at the time the invention was made for the reasons as given, and Official Notice is hereby taken.

Allowable Subject Matter

13. Claim 19-26 are allowable over the prior art of record due to the incorporation of the combination of features "asynchronously accessing the memory core more than once in a single clock cycle" in the independent claim.

14. Claim 27 is objected-to.

14. Claims 39, 40 and 43 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

15. Claims 38, 41, 42 and 44-49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Elmore whose telephone number is (703) 308-6256. The examiner can normally be reached on Mon-Fri from 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen Elmore
Assistant Examiner
Art Unit 2186

July 25, 2004